REMARKS

Status of Claims

Claims 1-15 are pending. Claims 1 and 7-9 are rejected. Claims 2-6 and 10-15 are objected to as being dependent upon a rejected base claim.

Claims 8, 11 and 14 have been amended to correct informalities in the claim language and to more clearly define the claimed subject matter. Claims 10, 12 and 15 have been amended to be rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 16 has been added to recite additional subject matter disclosed in the original specification that was not previously claimed. Claims 7 and 9 have been cancelled.

Rejection under 35 U.S.C. §102

Claim 1 is rejected under 35 U.S.C. §102(b) as being anticipated by Gowda et al. (USP 6,115,066). Applicant respectfully traverses this rejection for the following reasons.

The present invention relates to a solid state imaging device using N-type MOS transistors **alone** included therein as transistors, as recited by Claim 1. On the other hand, the image sensor of Gowda et al. relates to a CMOS image sensor where both N-MOS and P-MOS transistors are utilized. For example, a peripheral part of the image sensor includes a signal processing circuit, a timing and control logic circuit and a column select/scan logic which comprise CMOS circuits (see FIG. 3; col. 1, line 17 – col. 2, line 9; and col. 2, lines 61-65). Therefore, Gowda et al. fail to disclose a solid state imaging device using N-type MOS transistors **alone** as transistors.

As mentioned in the specification, an N-MOS solid state imaging device consisting of N-MOS transistors alone as transistors is expected to be a promising solid state imaging device that

can be fabricated through a significantly reduced number of processes necessary for forming wells and transistors in a substrate while keeping its imaging performance. According to the present invention, the N-MOS solid state imaging device has a rapid comparison/storage unit (thus, an A/D converter) consisting of N-MOS transistors alone and is capable of converting an analog signal output from the pixel unit into a digital format. Thus, the N-MOS solid state imaging device can attain an A/D conversion function equivalent to that of a CMOS solid state imaging device, utilizing only N-MOS transistors

Similar to Gowda, Kim et al. (USP 6,423,957) relates to a CMOS image sensor where a control and system interface unit and a reference voltage control unit comprises CMOS circuits (see Fig. 4; col.1, lines 5-32; col. 2, line 47 – col.3, line 3). Thus, Kim also fails to disclose an imaging device which utilizes only N-type MOS transistors.

Anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." ***Verdegaal Bros. v. Union Oil Co. of California***, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). For the reasons set forth above, the cited prior art does not disclose expressly or inherently the above recited limitation. Thus, Applicant respectfully requests that the Examiner withdraw the rejection of Claim 1. Since Claim 8 and the new claim 16 depend upon Claim 1, these claims are also allowable at least the same reason as Claim 1.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:TS:lcb
Facsimile: 202.756.8087
Date: August 8, 2007

Please recognize our Customer No. 53080 as our correspondence address.